CLAIMS

WHAT IS CLAIMED IS:

1. A bus bridge circuit, wherein the bus bridge circuit is adapted for coupling to a first bus comprising n address lines, and wherein n is an integer and $n \geq 2$, and wherein the bus bridge circuit comprises:

audio logic configured to access digital audio data and to produce an n-1 bit address when accessing the digital audio data; and

an addressable register comprising a bit position for storing an additional address bit; and

wherein when the audio logic is accessing digital audio data, the bus bridge circuit is configured to: (i) concatenate the additional address bit with the n-1 bit address to produce an n-bit address, wherein the additional address bit forms a most significant bit of the n-bit address, and (ii) drive the n-bit address upon the n address lines of the first bus.

2. The bus bridge circuit as recited in claim 1, wherein the addressable register has an address, and wherein a value may be stored in the addressable register via a write operation specifying the address of the addressable register.

3. The bus bridge circuit as recited in claim 1, wherein the n address lines of the first bus define an address space of the first bus, and wherein a bit stored in the bit position of the addressable register via a write operation determines whether the n-bit address resides in a

lower portion of the address space of the first bus, or in an upper portion of the address space of the first bus.

4. The bus bridge circuit as recited in claim 1, wherein the first bus is a peripheral component interconnect (PCI) bus having *n* multiplexed address/data lines.

5. The bus bridge circuit as recited in claim 1, wherein the bus bridge circuit is further adapted for coupling to a second bus, and wherein the bus bridge circuit is configured to translate signals between the first bus and the second bus.

6. The bus bridge circuit as recited in claim 5, wherein the first bus is a peripheral component interconnect (PCI) bus having *n* multiplexed address/data lines, and wherein the second bus is an industry standard architecture (ISA) bus.

7. The bus bridge circuit as recited in claim 1, wherein the audio logic is adapted for coupling to a speaker, and wherein the audio logic is configured to receive digital audio data, to transform the digital audio data to an analog signal, and to provide the analog signal to the speaker.

8. The bus bridge circuit as recited in claim 1, wherein the audio logic is adapted for coupling to a microphone, and wherein the audio logic is configured to receive an analog signal from the microphone, to transform the analog signal to digital audio data representing the analog signal, and to provide the digital audio data.

9. A computer system, comprising:

a first bus, wherein the first bus comprises n address lines, and wherein n is an integer and $n \geq 2$;

a bus bridge circuit coupled to the first bus, wherein the bus bridge circuit comprises:

audio logic configured to access digital audio data and to produce an n-1 bit address when accessing the digital audio data; and

an addressable register comprising a bit position for storing an additional address bit; and

wherein when the audio logic is accessing digital audio data, the bus bridge circuit is configured to: (i) concatenate the additional address bit with the n-1 bit address to produce an n-bit address, wherein the additional address bit forms a most significant bit of the n-bit address, and (ii) drive the n-bit address upon the n address lines of the first bus.

10. The computer system as recited in claim 9, wherein the addressable register has an address, and wherein a value may be stored in the addressable register via a write operation specifying the address of the addressable register.

11. The computer system as recited in claim 9, wherein the n address lines of the first bus define an address space of the first bus, and wherein a bit stored in the bit position of the addressable register via a write operation determines whether the n-bit address resides in a

lower portion of the address space of the first bus, or in an upper portion of the address space of the first bus.

12. The computer system as recited in claim 9, wherein the first bus is a peripheral component interconnect (PCI) bus having *n* multiplexed address/data lines.

13. The computer system as recited in claim 9, further comprising a second bus, wherein the bus bridge circuit is coupled between the first bus and the second bus, and wherein the bus bridge circuit is configured to translate signals between the first bus and the second bus.

14. The computer system as recited in claim 13, wherein the first bus is a peripheral component interconnect (PCI) bus having *n* multiplexed address/data lines, and wherein the second bus is an industry standard architecture (ISA) bus.

15. The computer system as recited in claim 9, wherein the audio logic is adapted for coupling to a speaker, and wherein the audio logic is configured to receive digital audio data, to transform the digital audio data to an analog signal, and to provide the analog signal to the speaker.

16. The computer system as recited in claim 9, wherein the audio logic is adapted for coupling to a microphone, and wherein the audio logic is configured to receive an analog signal from the microphone, to transform the analog signal to digital audio data representing the analog signal, and to provide the digital audio data.

17. A computer system, comprising:

a first bus comprising *n* address lines, wherein *n* is an integer and $n \geq 2$;

a second bus;

a bus bridge circuit coupled between the first bus and the second bus, wherein the bus bridge circuit is configured to translate signals between the first bus and the second bus;

wherein the bus bridge circuit comprises:

audio logic configured to access digital audio data and to produce an *n*-1 bit address when accessing the digital audio data; and

an addressable register comprising a bit position for storing an additional address bit, wherein the addressable register has an address, and wherein a value may be stored in the addressable register via a write operation specifying the address of the addressable register; and

wherein when the audio logic is accessing digital audio data, the bus bridge circuit is configured to: (i) concatenate the additional address bit with the *n*-1 bit address to produce an *n*-bit address, wherein the additional address bit forms a most significant bit of the *n*-bit address, and (ii) drive the *n*-bit address upon the *n* address lines of the first bus.

18. The computer system as recited in claim 17, wherein the n address lines of the first bus define an address space of the first bus, and wherein a bit of a value stored in the bit

position of the addressable register via a write operation determines whether the *n*-bit address resides in a lower portion of the address space of the first bus, or in an upper portion of the address space of the first bus.

19. A method for initializing a chip set of a computer system, wherein the chip set comprises a bus bridge circuit coupled to a bus and includes audio logic and an addressable register, and wherein the addressable register comprises a bit position providing an additional address bit, and wherein the bus bridge circuit produces addresses when the audio logic accesses digital audio data, and wherein the additional address bit forms a most significant bit of the addresses, the method comprising:

initializing the bit position of the addressable register to a default value; and

changing the value of the bit position of the addressable register if the default value will cause the bus bridge circuit to produce addresses which do not reside in a target portion of the address space of the bus when the audio logic accesses digital audio data.

20. The method as recited in claim 19, wherein changing the value of the bit position causes the target portion of the address space of the bus to be either: (i) a lower half of the address space of the bus, or (ii) an upper half of the address space of the bus.

21. The method as recited in claim 19, wherein initializing comprises:

initializing the bit position of the addressable register to a logic '0' default value.

22. The method as recited in claim 21, wherein changing comprises:

changing the value of the bit position of the addressable register to a logic '1' if the logic '0' default value will cause the bus bridge circuit to produce addresses which do not reside in a target portion of the address space of the bus when the audio logic accesses digital audio data.

23. A carrier medium comprising program instructions for initializing a chip set of a computer system, wherein the chip set comprises a bus bridge circuit coupled to a bus and including audio logic and an addressable register, and wherein the addressable register comprises a bit position providing an additional address bit, and wherein the bus bridge circuit produces addresses when the audio logic accesses digital audio data, and wherein the additional address bit forms a most significant bit of the addresses, and wherein the program instructions are operable to implement:

initializing the bit position of the addressable register to a default value; and

changing the value of the bit position of the addressable register if the default value will cause the bus bridge circuit to produce addresses which do not reside in a target portion of the address space of the bus when the audio logic accesses digital audio data.

24. The carrier medium as recited in claim 23, wherein the carrier medium is a computer-readable storage medium.

25. The carrier medium as recited in claim 24, wherein the computer-readable storage medium is a floppy disk or a compact disk read only memory (CD-ROM) disk.